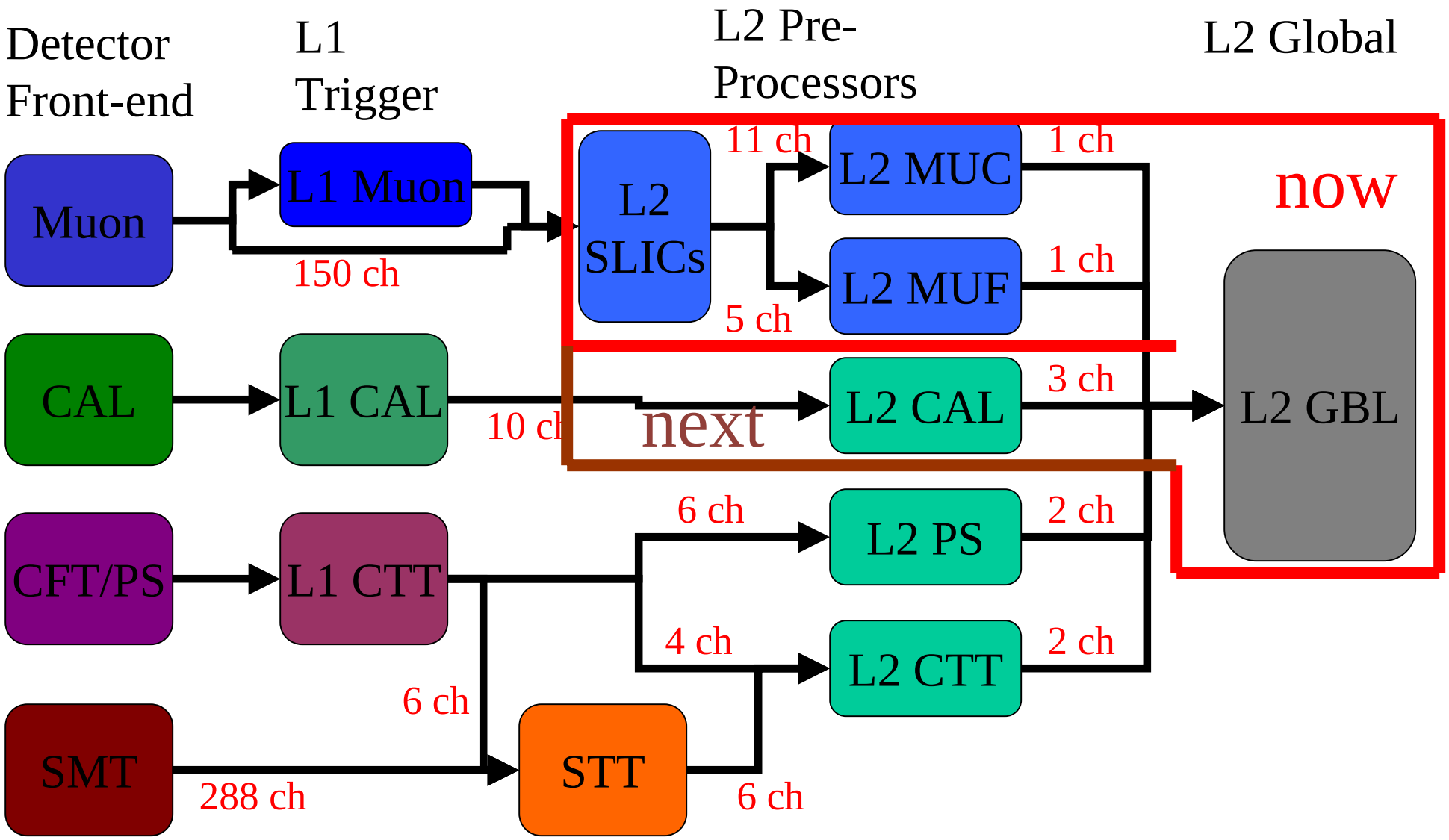
Reinhard Schwienhorst
for the DØ L2 group

AEM 05/13/02

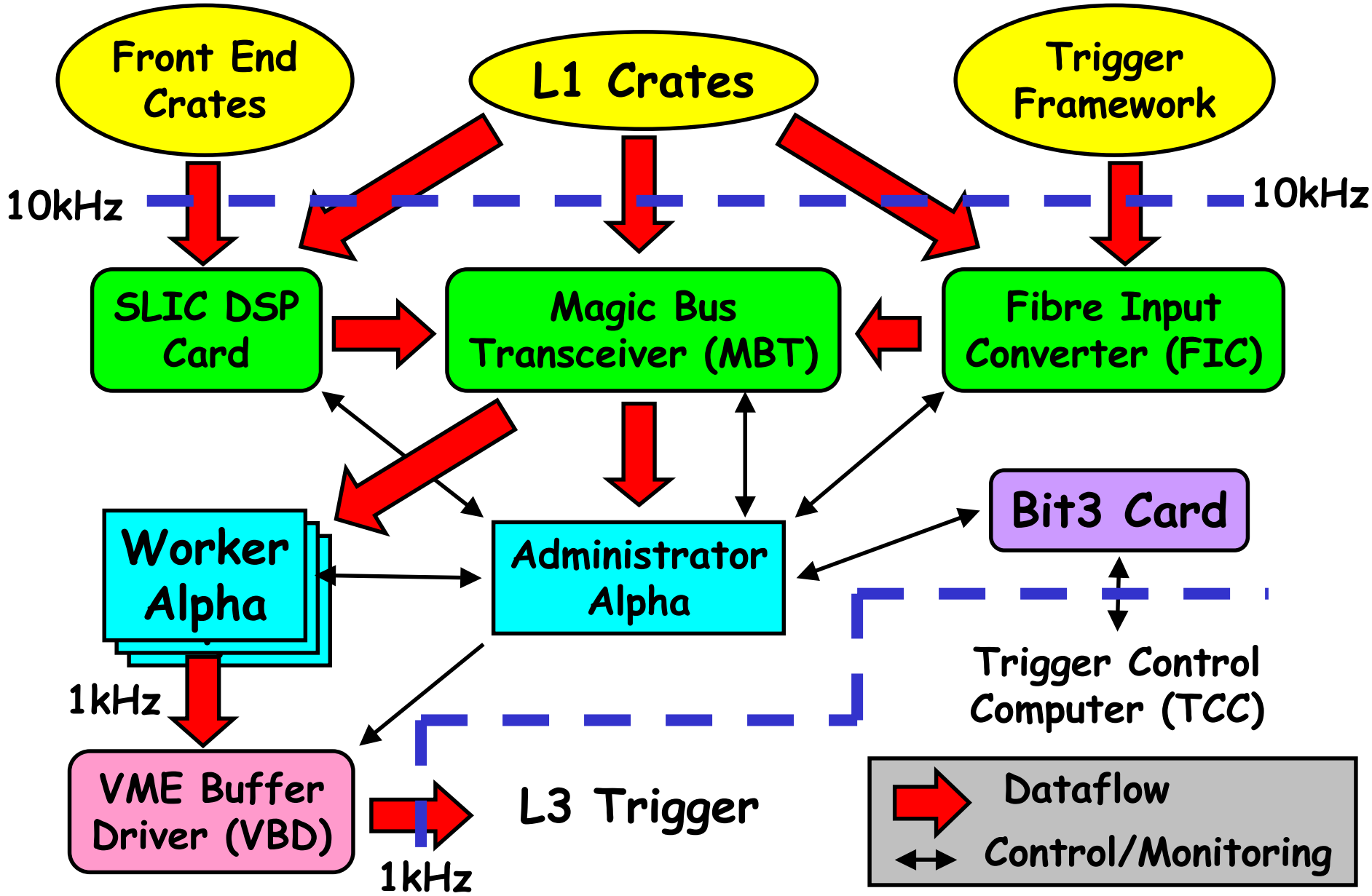
Outline

- L2 Trigger dataflow
- L2 Crate
- Current L2 setup
- L2 Muon
- L2 Cal
- L2 Plans

L2 Trigger Dataflow



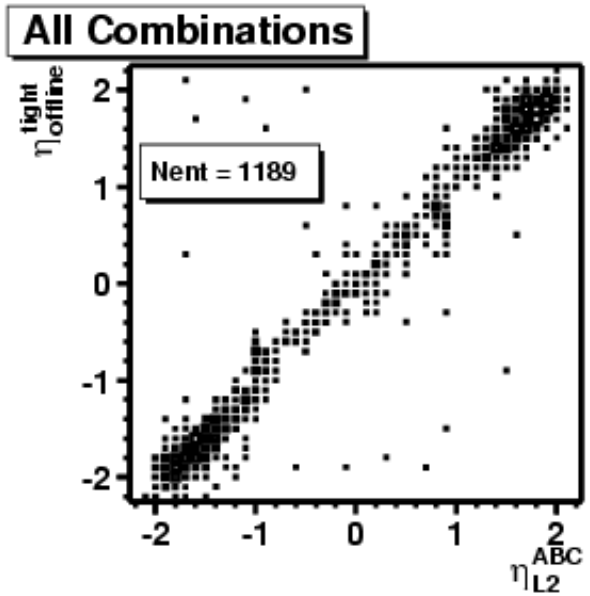
L2 Crate

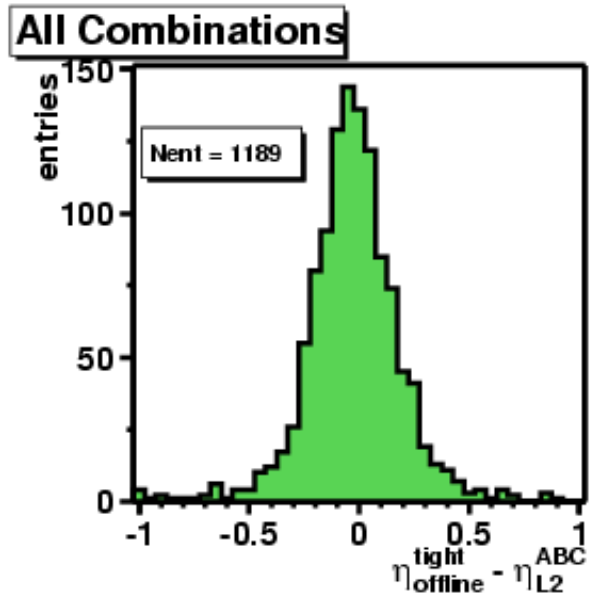

Front End Crates
L1 Crates
Trigger Framework
10kHz
10kHz
SLIC DSP Card
Magic Bus Transceiver (MBT)
Fibre Input Converter (FIC)
Bit3 Card
Worker Alpha
Administrator Alpha
Trigger Control Computer (TCC)
1kHz
VME Buffer Driver (VBD)
1kHz
L3 Trigger
Dataflow
Control/Monitoring

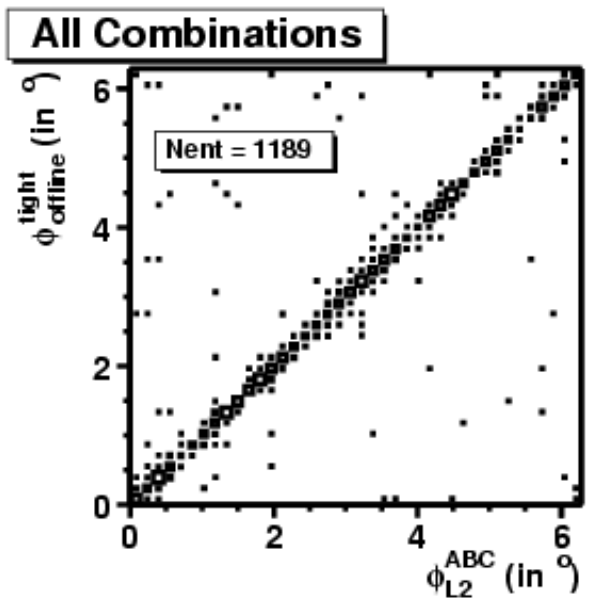
Current L2 Setup

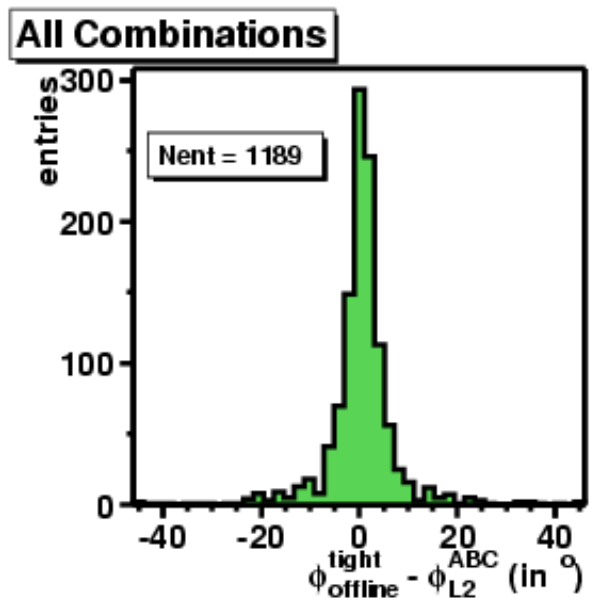
- Reject on loose muons
  - 2 identical L1 trigger bits
    - Adjust prescales to get effective rejection
  - Rejection factor (L1/L2) ~1.6 for muon bits
- 1 Alpha per pre-processor crate
  - Problem: Alpha PIO firmware, Mbus arbitration
  - Administrator and Worker combined
    - CAL: EM and Jet worker combined
  - Input rate limit ~ 2kHz

Muons: L2 vs Reco



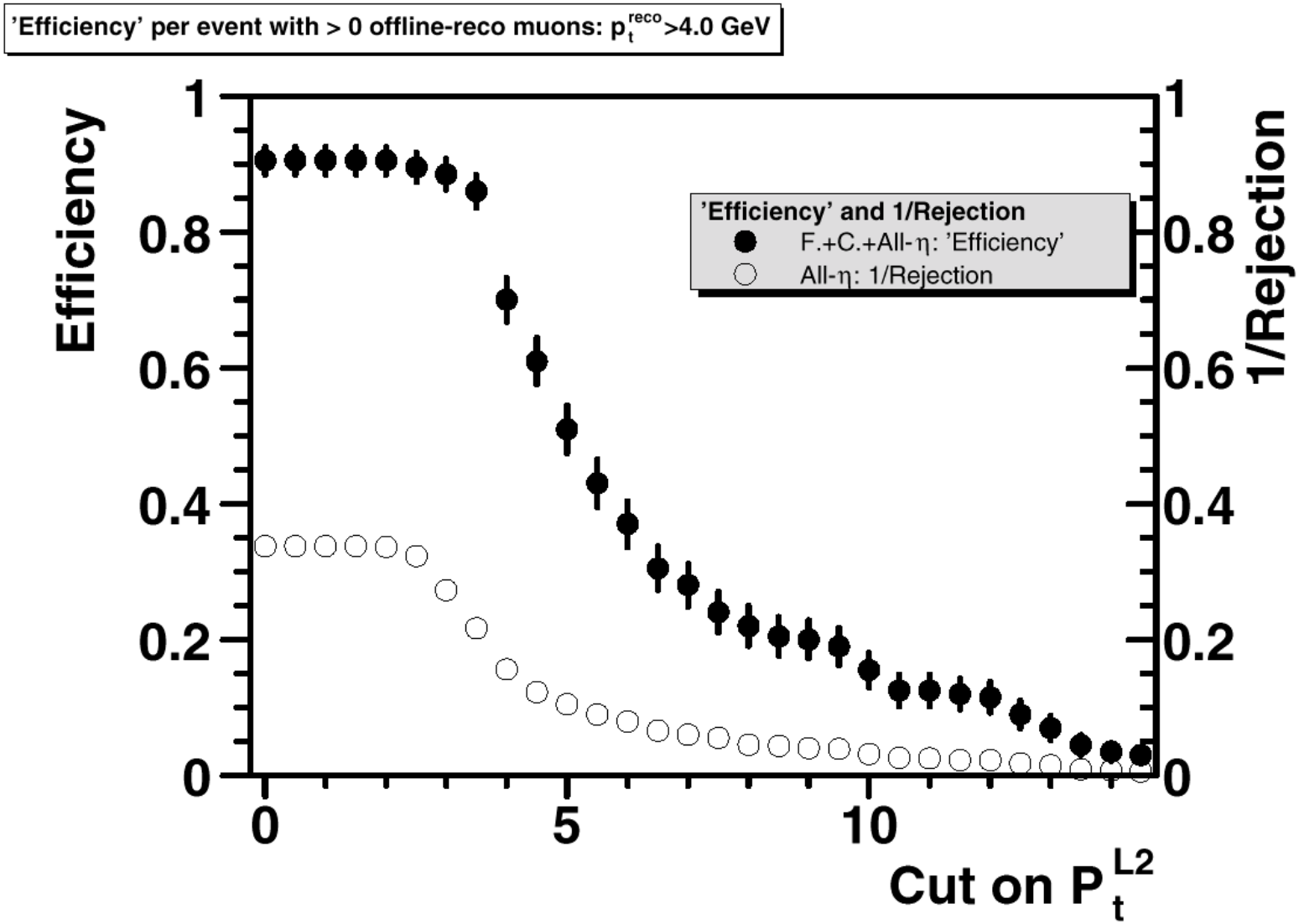




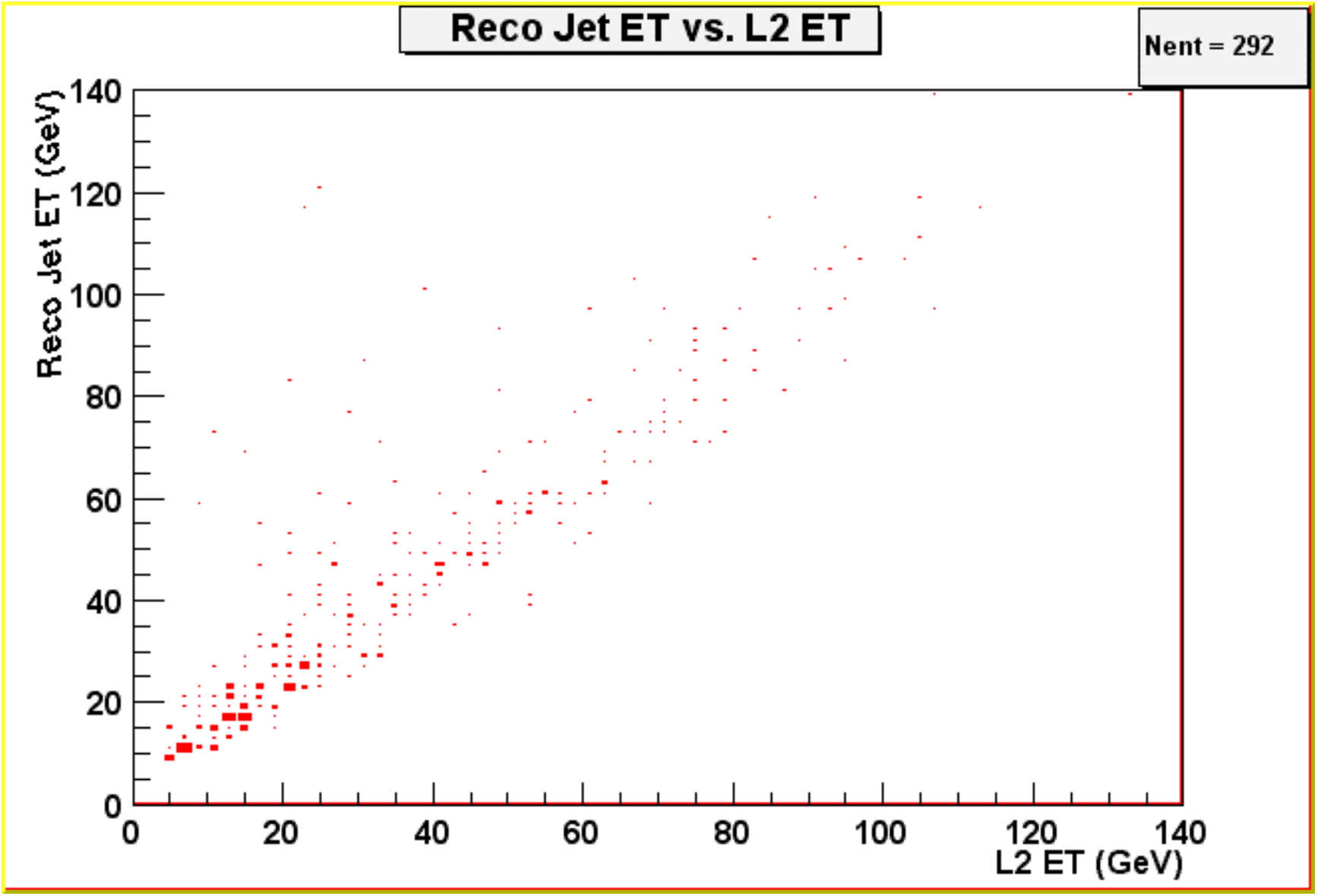


(η, φ) correlation for tight off-line muons and medium L2MU (matched A&BC stubs)

L2 Muon Rejection



Cal Jet: L2 vs Reco



L2 Plans

- Near-term future:
  - Muon P_T cut
  - CAL cuts
    - jets: cluster L1CAL towers
    - EM: EM fraction cut on L1CAL towers
- Mid-term future:
  - Add L2CTT and L2PS
    - When inputs become available
  - Multiple Alphas in a few crates
- Long-term future:
  - Beta processors
  - STT